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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,242	02/06/2004	Chang-Ho Cho	2557-000190/US	6461
30593	7590	05/03/2006	EXAMINER	
HARNES, DICKEY & PIERCE, P.L.C.			DAVIS, ROBERT B	
P.O. BOX 8910			ART UNIT	
RESTON, VA 20195			PAPER NUMBER	

1722

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/772,242	Applicant(s) CHO, CHANG-HO	
	Examiner Robert B. Davis	Art Unit 1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-16 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/28/05, 2/6/4</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue (JP 11-176855 A: figures 1-5 and abstract).

Inoue teaches a mold die for encapsulating a semiconductor device comprising; a cavity block having a plurality of cavities (figure 4) in which a chip is positioned, a gate (8a) defining a resin entry into the mold cavity and having a gate width, a gate block (8) arranged for relative movement with the mold cavity to allow opening and closing of the gate (see figures 1-open and figure 3-closed), wherein the gate is arranged at a 45 degree to the sides of the mold cavity. It is inherent that the gate is positioned at an angle of less than 90 degrees with respect to the chip.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue taken together with Shibata (5,750,153: figures 1-15 and column 1, lines 21-36).

Inoue discloses all claimed features except for the die having a channel block. The reference does disclose a plurality of pots (6) for storing and injecting resin with a ram.

Shibata disclose a mold die for packaging/encapsulating a semiconductor chip comprising: upper and lower cavity blocks (5D, 5C), a gate block (6C) and a runner or channel block (59) for distributing resin from a central source to a plurality of molding cavities.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Inoue by providing a cavity block to supply a plurality of molding cavities with resin from a common source as disclosed by Shibata because such a separate channel block allows for replacement of individual parts without replacing the entire mold die. It is further obvious to use a channel system for supplying a plurality of mold cavities with resin from a central source as disclosed by Shibata because such a configuration reduces the amount of pots and plungers and thus reduces the amount of resin tablets supplied per molding operation by reduction of the number of pots.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue taken together with Shin et al (6,717,248: figures 12B and 13, and column 12, lines 45-67).

Inoue discloses all claimed features except for the use of a L-gate having two surfaces parallel with two sides of the chip.

Shin et al disclose an apparatus for packaging a semiconductor chip (2) having a gate (G) having a L-shaped gate (H) as illustrated in figure 12B.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the apparatus of Shin et al by having a L-shaped gate for the purpose of matching the gate shape to the edge of the chip.

6. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue taken together with Shibata.

Inoue discloses a method of encapsulating a semiconductor chip using a mold having a gate block that is movable to close the gate after injecting resin into the mold cavity as described earlier in this action. The abstract and drawings are silent as to the orientation of the chip in relation to the molding cavity.

Shibata disclose a method of packaging/encapsulating a chip (3) in a molding cavity (50), wherein the chip is square and arranged such that the sides of the chip are parallel to the molding cavity surfaces see figure 1. The resin is introduced at a corner of the cavity by means of a gate (29) such that the resin approaches the sides of the chip (3) at an angle of less than 90 degrees.

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the method of Inoue by orienting the chip such that the sides of the chip are parallel to the sides of the molding cavity as disclosed by Shibata for the

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purpose of positioning the chip within the molding cavity such that the package resin has the same thickness on each side of the chip.

Claim Objections

7. Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 11 only further limits the chip, which may be positioned within a mold cavity. Since claim 10 does not positively recite the chip as a structural element, further limiting the chip in claim 11 does not further limit the structure of claim 10.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is indefinite because the gate width is not clear. It is unclear what gate width is defined by the phrase "the gate width is at least equal to one-half of a first length equal to the shorter of the third and fourth side wall segments and is less than second length equal to the longer of the third and fourth side wall segments."

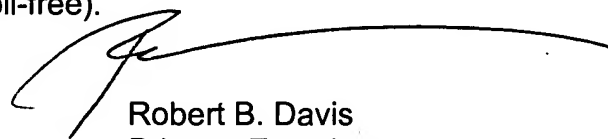
Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The remaining references illustrate the state of the art of packaging molds for semiconductor chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Davis whose telephone number is 571-272-1129. The examiner can normally be reached on Monday-Friday 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Robert B. Davis
Primary Examiner
Art Unit 1722

5/1/06